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**PATENT**  
Attorney Docket No.: 020937-000610US  
Client Ref. No.: HARI 006UST

Assistant Commissioner for Patents  
Washington, D.C. 20231

On October 31, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: James Curran-Cass

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

ELIYAHOU HARARI et al.

Application No.: 09/143,233

Filed: August 28, 1998

For: FLASH EEPROM SYSTEM  
WITH DEFECTIVE BLOCK  
SUBSTITUTION (as amended)

Examiner: Hien Nguyen

Art Unit: 2824

AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

In response to the office action mailed October 1, 2001, please amend the above-identified application as follows:

IN THE SPECIFICATION:

At page 5, please replace the paragraph beginning on line 27 with the following:

Fig. 8 is a block diagram illustrating the write cache circuit inside the controller;

Fig. 9 outlines the key steps in the new algorithm used to erase with a minimum stress;

207# Amended  
TECHNOLOGICAL CENTER 2800  
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